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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptonotifs@yeeiplaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/675,776	DEWITT ET AL.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6 and 26-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 6, 26-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 3/20/08.

As indicated in Applicant's response, claim 32 has been amended. Claims 1-2, 6, 26-48 are pending in the office action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 21, 25 of copending Application No. 10/675777 (hereinafter '777).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per instant claims 1, 32, 41, '777 claims 6, 21, 25 also recite determining for a instruction during execution for a association of an indicator associated with receiving a bundle or instruction in a instruction cache; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction or event associated with the indicator. The event counting and instruction cache as recited by '777 are construed as obvious representation to a runtime indicator (leading to a counter increment, in which incrementing is count of number of instructions execution) and sending from the cached instruction for execution of the instant claims.

4. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 10, 20 of copending Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per claims 1, 32, 41, '778 claims 2, 10, 20 recite receiving a instruction with an indicator generated from a instruction cache, wherein upon determining that an indicator is associated with an instruction and a signal from the cache instruction, incrementing the counter each time the instructions is executed based on said cache signal. Even though '778 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, this limitation of instruction associated with indicator from cache would made the sending a obvious step within runtime based on instruction being cached in view of the above association and counting event.

5. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 32, 41, '872 claims 3, 17 also recite instruction to be monitored and sent from cache instruction, determining whether an instruction in execution is related with an runtime range 'indicator'; and counting each event associated with the instruction if the instruction is associated with that range indicator. Even though '872 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing in terms of count of number of instructions execution) in view of the above association determination.

6. Claims 6, 34, 43 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 12, 20 of copending Application No. 10/675721 (hereinafter '721).

As per instant claims 6, 34, 43, '721 claims 4, 12, 20 also recite determining for a instruction during execution for a association of a indicator, shadow memory (Note: even though '721 does not recite counter in shadow memory per se, a set of indicators being sent for

monitoring would have made the counter as obviously in the shadow memory); incrementing a counter in response to the indicator association with the instruction, and responsive to which, executing while incrementing said executing. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '721 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. The instruction in the *routine of interest* as recited by '721 is construed as obvious representation to a runtime instruction that requires some action (e.g. to monitor or to trace/modify leading to a counter increment in which incrementing is in terms of count of number of executions) of the instant claims.

7. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12, 23 of copending Application No. 10/682385 (hereinafter '385).

As per instant claims 1, 32, 41, '385 claims 1, 12, 23 also recite executing instructions and detecting indicators that specify counting of events associated with the executing (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with indicators. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '385 does not recite receiving bundle into a instruction cache and sending the received bundle for

execution, said limitation of executing instructions associated with indicators would made the instruction cache reception and the sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '385 explicitly recites that counting events associated with execution based on detection of value indicators, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of executions) in view of the above association determination.

Specification

8. The amendment filed 3/20/08 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: a) 'determination is made in instruction cache' (original: 'When instruction cache determines'); b) 'may be implemented in conjunction with an instruction cache' (original: 'implemented in an instruction cache') (pg. 23, li 17: pg. 32, li. 6; pg 34, li. 14). Applicant is advised that, for one of ordinary skill in the art, there is a difference between *implemented within* hardware unit and *implemented in conjunction with* such. Clarification as to how the above added language a) and b) to the Specifications had been taught in the original Disclosure is required. Otherwise, Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-2, 6, 26-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gover et al., USPN: 5,752,062(hereinafter Gover) in view of APA (Admitted Prior Art: Specifications: Description of Related Art, pg. 2-3).

As per claim 1, Gover discloses a method in a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle, the bundle containing an instruction (e.g. Fig. 1; Fig. 3);

responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator (see col. 7, lines 15 to col. 7, lines 17) identifies the instruction as one that is to be monitored by a performance monitor unit (Fig. 5);

responsive to a determination that the bundle contains the indicator, incrementing a counter (e.g. Fig. 5; col. 7, line 62 to col. 8, line 17) associated with the instruction wherein the incrementing providing provides a count of a number of times the instruction is executed (see Fig. 6a, 6b); and

sending the bundle to a functional unit for execution of the instruction (col. 4, lines 44-49).

Gover does not explicitly disclose 'instruction cache' unit that *receives the bundle, determine the instruction to be counted based on the indicator for monitoring, and sending the bundle from the ICU to the execution unit*; that is, not implementing the instruction cache, the sequence unit (see Fig. 1) and the monitoring unit (Fig. 2; Fig. 4; col. 7, lines 15 to col. 7, lines 17) in a combined functional unit such as a single instruction cache unit (ICU). Gover discloses bus interface between instruction cache and sequencer unit (see Fig. 1; col. 6, lines 7-20); sequencer unit depending on *rename buffer* interface (col. 6, lines 13-19); dispatching process including associating completion/allocation interfaces (e.g. Fig. 3) for updating information (or indicators) in a reorder buffer in terms of conditions (see *finished, exception* - col. 6, line 66, to col 7, line 2) based on which some monitoring action (e.g. condition 2 - col. 10, line 9-12; dispatch logic 74 - Fig. 2; col. 7, lines 15 to col. 7, lines 17) can be applied; that is, using the performance monitor unit, in conjunction with the special registers or MMCRn (e.g. Fig. 4; Fig. 5; Fig. 6a). The meta-information being dispatched from the bundle of instructions coming from the reorder buffer, sequencer, rename buffer, and the tight relationship thereof with the original instruction cache (Fig. 1) and the performance monitor by Gover entails that the dispatched bundle contains instructions or data back and forth between cache and hardware monitoring tool. APA teaches combining hardware performance tools (Specifications, pg. 3) into a software application performance system or a trace tool using profiling. In view of the role played by the MMCRn and the sequencer, the cache interface unit, a rename process and the handling of runtime exception based on the hardware monitoring role as in Gover, i.e. the interdependency of functionality (hardware and software) units involved, it would have been obvious for one skill in the art at the time the invention was made to implement Gover's instruction cache, sequencer

unit and monitoring unit (*performance monitor 50*, Fig. 4 –i.e. hardware tools) as one functionality called *instruction processing unit* -- or more arbitrarily a 'instruction cache', or ICU- to effectuate a performance monitoring/support functionality such as contemplated by APA in terms of faster hardware performance. That is, one would be motivated to do so because this ICU can be called upon to **receive bundle**, trigger **monitoring event** based on indicators set forth by the reorder buffer inside the sequencer unit and provide expedite monitoring action (based on hardware support) operating on data from the dispatched bundle and based on the dynamic condition/state (e.g. *exception, finished, completion*) indicated by the bundle as set forth above (Fig. 6a, 6b) then accordingly **send the bundle** for execution after the appropriate monitoring action has taken place; and therefore enable the ICU to tackle problem based on state knowledge, e.g. completed state of an dispatched instructions (see col. 7, line 44 to col 7, line 17; col. 15, line 36 to col. 16, line 22) in a timely manner without delays that would have resulted in cache miss (see col. 16, line 59 to col. 17, line 67)

As per claim 2, Gover discloses resetting the counter if the counter exceeds a threshold value; and reading a value of the counter prior to the counter exceeding the threshold value (e.g. *reset* - col. 12, lines 4-42)

As per claim 6, Gover discloses wherein the counter is located in a shadow memory (col. 8, lines 26-39 – Note: special registers and PMCs with state or content – MMCRn -- maintained via special privilege access mode and being kept in parallel with execution scheduling – see col. 11, lines 14-50 -- as informational support thereof, hence reads on shadowing type of information kept in memory; see SSR col. 9 lines 36-57).

As per claim 26, Gover does not explicitly disclose comprising using a spare field in the bundle to contain the indicator; but based on the indicators received by the execution unit sent by the sequencer and based on which to execute some needed performance monitoring action (see Fig. 6a-b), it would have been obvious for one skill in the art at the time the invention was made to enable a special field in the bundle as set forth in claim 1 so that a spare slot contains this indicator, among the other slots that are primarily allotted for the instruction per se (see Fig. 3)

As per claim 27-28, Gover discloses responsive to a determination that the bundle contains the indicator, sending a signal to the performance monitor unit (interrupt - col. 9, lines 30 to col. 10, line 5; Fig. 7); wherein the step of incrementing the counter (e.g. col. 10, lines 40-63) associated with the instruction is performed by the performance monitor unit.

As per claim 29, Gover discloses responsive to a determination that the bundle contains the indicator, beginning incrementing the counter, wherein the counter (refer to claim 27-28) tracks any subsequent instruction executed by an associated processor (e.g. *to correspond to a particular processor* – col. 8, lines 46-55).

As per claims 30-31, Gover does not disclose receiving a second bundle at the instruction cache; responsive to receiving the second bundle, determining whether the second bundle contains a second indicator; and responsive to a determination that the second bundle contains the second indicator, ending incrementing the counter. But the ICU for receiving, determining responsive to an indicator has been addressed in claim 1; and in light of the subsequent incrementing for monitoring an event (see claim 29), Gover discloses wherein the counter and the second counter are identical. For the second indicator, however, based on the providing of stop point in the hardware monitoring registers as by Gover (*stop point* – col. 10,

lines 1-16; *threshold value* – col. 10, lines 40-66) where some indicators can be adjusted, it would have been obvious for one skill in the art at the time the invention was made to implementing monitoring unit by Gover so that when a second bundle contains a stop point or a threshold being reached or exceeded, some counting would have to be stopped for an corrective action to take place.

As per claim 32, Gover discloses computer program product, comprising:

a computer readable recordable-type medium having computer useable program code for monitoring execution of instructions, the computer program product comprising code for performing the steps of:

receiving a bundle…;

determining whether …indicator …;

incrementing … ;

sending … for execution;

all of which have been addressed in claim 1, incorporating thereby the rationale as to render the 'instruction cache' (for receiving determining incrementing and sending) limitation obvious as set forth therein.

As per claims 33-34, refer to claims 2, 6 respectively.

As per claims 35-40, refer to claims 26-31, respectively.

As per claim 41, Gover discloses a data processing system comprising:

a bus; a communications unit connected to the bus; a storage device connected to the bus, wherein the storage device includes computer usable program code; and a processor unit connected to the bus (Fig. 1), wherein the processor unit executes the computer usable program code to:

receive a bundle…;

determine whether …indicator …;

increment … ;

send … for execution; all of which have been addressed in claim 1, incorporating thereby the rationale as to render the 'instruction cache' (for receiving determining incrementing and sending) limitation obvious as set forth therein.

As per claims 42-48, refer to claims 33-39, respectively.

Response to Arguments

11. Applicant's arguments filed 3/20/08 have been fully considered but they are not persuasive. Following are the Examiner's observation in regard thereto.

35 USC § 103 Rejection:

(A) Applicants have submitted that none of the portions cited in Glover (col. 3, 8, 9) by the Office Action discloses 'responsive to receiving a bundle, determining whether ... indicator identifies the instruction as one that is to be monitored ... by the performance monitor unit' (Appl. Rmrks, pg. 15, bottom) because Gover merely teaches indicating of instruction to be dispatched from the reorder buffer. The rationale of rejection is to address using a hardware based unit in conjunction with a instruction cache, reorder buffer, sequencer and performance monitor to monitor events based on indicators (see reorder buffer state: exception, finished, completion – col. 7 lines 25-61) as taught by Gover to support Gover's dynamic non-intrusive monitoring process in terms of determining which instructions to monitor, counted and dispatched. The cited portions are not used to anticipate the language of the limitation claimed as 'responsive to receiving a bundle, determining whether ... indicator identifies the instruction

as one that is to be monitored ... by the performance monitor unit', but are actually laid out to establish context and purpose in the teachings in a reference to support how as combined according to knowledge of one of ordinary skill in the art would fulfill the above limitation, in light of APA. The steps sequenced in the claim entails a combination of hardware units operating together (emphasis added) in order to determine which instruction to dispatch instruction from a cache to a runtime engine. The motivation has been set forth in the Office Action rationale, in light of Gover's endeavor and known practice using hardware to support monitoring of selected instructions during execution. The argument appears to dissect each cited portions proffered in a USC § 103 rationale as though the portions are for effectuating a USC 102 rejection. The argument is not commensurate with the grounds and specifics of the rationale effectuated in the Office Action. The grounds provided by the Applicants are deemed insufficient in showing by facts how the teachings by Gover, in light of APA cannot be modified so as to fulfill one particular feature of the claim which has been interpreted and addressed as following: using a combination of hardware-based unit that would operated as a single operational unit to determine, based on some indicator, which instructions to monitor or count prior to its execution from an instruction cache. The argument fails to point out **where** exactly the specifics (e.g. the hardware units by Gover in view of the communication of events based on the reorder buffer) provided in the 103 rationale is teaching away against the endeavor by Gover or APA, or would, even as combined, fail to effectuate the functional aspect of very language of such limitation. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based

on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(B) Applicants have submitted that prima facie rejection has not been provided by the Examiner and for claim 1, as well as for claims 6, 26-31, 32, 41, 33-40, rejection should be withdrawn. The arguments as provided above are not deemed sufficient to overcome how one (of ordinary skill in the art) would be motivated to combine the flow of interdependency of data in Gover's reorder buffer, scheduler, performance monitor unit with APA (using hardware to capture selective instructions for monitoring purpose) in order to use the indicators in the reorder buffer to determine which cached instructions to be monitored when these instructions are dispatched for execution.

USC 35 § 112 Rejection:

(C) Applicants have modified the Specifications from a 'cache determines' to 'determination is made' and from 'implemented by a instruction cache' to 'in conjunction with a instruction cache' (refer to: Specifications: Objections); and this added subject matter raises a question as to whether this subject matter is reasonably present in the original Specifications. Applicants have in the one hand stated that, contrary to the Examiner's narrow view, an *instruction cache subsystem* would include 'cache controller', according to broad interpretation in the art (Appl. Rmrks, pg. 11, middle); and on the other hand, have modified the Specifications to above extent, e.g. change the Specifications from a feature reciting determination made in a instruction cache to determination made whether a indicator is present in the cache (see Specifications: pg. 23, li 17). Based on the above mutually exclusive presentation of facts, Applicants are urged to provide (i) concrete evidence that any cache *subsystem* **inherently includes** a *cache controller*

having itself a determination functionality; and (ii) how a cache unit that was originally disclosed as 'instruction cache determines if an instruction associated with an indicator is present' **can be now same as** 'determining is made that an instruction associated with an indicator is present in instruction cache". Pending further rebut from the Applicants, the USC 112 Rejection previously raised is now replaced by an objection in form of introduction of new matter in the Disclosure. The prior-art rejection as set forth in the Office Action is maintained based on the understanding that the changes to the Specifications are not entered.

In all, the claims will stand rejected as set forth in the Office Action.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571)272-3759.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan A Vu/

Primary Examiner, Art Unit 2193

June 10, 2008